FEATURES

- 10-Bit Resolution
- Full Four-Quadrant Multiplication
- Nonlinearity: 1/2 or 1 LSB
- TTL/CMOS Compatible
- Improved Gain Error and Linearity Error from +5V to +15V
- Low Power Consumption
- Low Feedthrough Error
- Low Cost
- AD7520 and AD7533 Replacement
- Full Temperature Operation
- Improved ESD Protection
- Available in Die Form

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Gain Amplifiers
- Ratiometric A/D Conversion
- Function Generator
- CRT Graphics Generator
- Digitally-Controlled Attenuator
- Digitally-Controlled Power Supplies
- Digital Filters
- Linear Automatic Gain Control

ORDERING INFORMATION †

	PACKAGE		
NONLINEARITY	MILITARY* TEMPERATURE −55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±0.05% (±1/2 LSB)	PM7533AQ	PM7533EQ	PM7533GP
±0.1% (±1 LSB)	PM7533BQ	PM7533FQ	–
±0.1% (±1 LSB)	–	PM7533FP	–
±0.1% (±1 LSB)	–	PM7533FPC	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7533AQ	AD7533UD	MIL
PM7533BQ	AD7533TD	
PM7533BQ	AD7533SD	
PM7533EQ	AD7533CD	IND
PM7533FQ	AD7533BD	
PM7533FQ	AD7533AD	
PM7533GP	AD7533LN	COM
PM7533FP	AD7533LN	
PM7533FPC	AD7533KP	

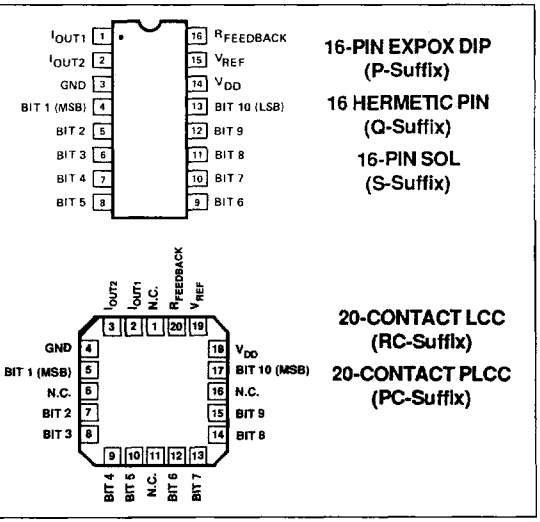
GENERAL DESCRIPTION

The PM-7533 is a 10-bit 4-quadrant multiplying DAC. It is manufactured using thin film on an oxide-isolated, silicon-gate, monolithic CMOS wafer fabrication process. PMI's advanced thin-film resistor processing provides true 10-bit linearity and excellent long-term stability without laser trimming.

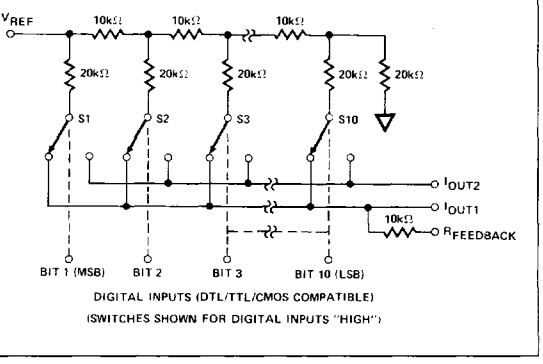
The PM-7533 is pin and function equivalent to the AD7520 and AD7533.

The PMI PM-7533 applications flexibility allows direct interface to TTL or CMOS circuitry and operation from +5V to +15V power supplies. Output scaling is provided by the internal feedback resistor and an external op amp; both positive and negative reference voltages can be accommodated.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} (to GND) ..... −0.3V, +17V
V_{REF} (to GND) ..... ±25V
R_{FB} (to GND) ..... ±25V
Digital Input Voltage Range ..... −0.3 to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... −0.3 to V_{DD}
Operating Temperature Range
Military (AQ, BQ Versions) ..... −55°C to +125°C
Industrial (EQ, FQ, FP, FPC) ..... −40°C to +85°C
Commercial (GP Version) ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC, TC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener protected, however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, T_A = −55°C to +125°C apply for PM-7533AQ/BQ, T_A = −40°C to +85°C apply for PM-7533EQ/FQ/FP/FPC/FS, T_A = 0°C to +70°C apply for PM-7533GP, unless otherwise noted.

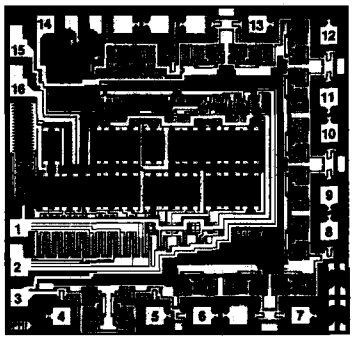
PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G MIN	PM-7533A/E/G TYP	PM-7533A/E/G MAX	PM-7533B/F/H MIN	PM-7533B/F/H TYP	PM-7533B/F/H MAX	UNITS
STATIC ACCURACY									
Resolution	N		10	—	—	10	—	—	Bits
Relative Accuracy (Note 1)	INL		— —	— —	±0.05 (±1/2)	— —	— —	±0.1 (±1)	% FSR (LSB)
Differential Nonlinearity (Note 12)	DNL		— —	— —	±0.1 (±1)	— —	— —	±0.1 (±1)	% FSR LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	— — — —	— — — —	±1.4 (±14) ±1.5 (±15)	— — — —	— — — —	±1.4 (±14) ±1.5 (±15)	% FS (LSB) % FS (LSB)
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$ (Note 4)	PSRR	T_A = +25°C T_A = Full Temp. Range	— —	— —	0.005 0.008	— —	— —	0.005 0.008	%/%
Output Leakage Current I_{OUT1} (Pin 1) (Note 6)	I_{LKG1}	T_A = +25°C T_A = Full Temp. Range	— —	— —	±50 ±200	— —	— —	±50 ±200	nA
Output Leakage Current I_{OUT2} (Pin 2) (Note 7)	I_{LKG2}	T_A = +25°C T_A = Full Temp. Range	— —	— —	±50 ±200	— —	— —	±50 ±200	nA
DYNAMIC ACCURACY									
Output Current Settling Time (Notes 5, 8)	t_S	T_A = +25°C (Note 10) T_A = Full Temp. Range	— —	— —	600 800	— —	— —	600 800	ns
Feedthrough Error (Notes 5, 10)	FT	T_A = +25°C T_A = Full Temp. Range	— —	— —	±0.05 ±0.1	— —	— —	±0.05 ±0.1	% FSR
REFERENCE INPUT									
Reference Input Resistance (Pin 15) (Note 11)	R_{IN}		5	—	20	5	—	20	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = V_{INH}	— —	— —	100 35	— —	— —	220 60	pF
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = V_{INL}	— —	— —	60 100	— —	— —	120 165	pF

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, T_A = –55°C to +125°C apply for PM-7533AQ/BQ, T_A = –40°C to +85°C apply for PM-7533EQ/FQ/FP/FPC/FS, T_A = 0°C to +70°C apply for PM-7533GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G MIN	PM-7533A/E/G TYP	PM-7533A/E/G MAX	PM-7533B/F MIN	PM-7533B/F TYP	PM-7533B/F MAX	UNITS
DIGITAL INPUTS									
Digital Input High	V_{INH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V_{INL}		—	—	0.8	—	—	0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V and V_{DD}	—	—	±1	—	—	±1	µA
Input Capacitance (Note 5)	C_{IN}		—	—	10	—	—	10	pF
POWER REQUIREMENTS									
Power Supply Voltage	V_{DD}		—	—	+15 ±10%	—	—	+15 ±10%	V
Power Supply Voltage Range	PSR	Accuracy is not guaranteed over this range	+5	—	+16	+5	—	+16	V
Supply Current	I_{DD}	Digital inputs = V_{INL} or V_{INH}	—	—	2	—	—	2	mA

NOTES:
1. "FSR" is full-scale range.
2. Full-scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$; Digital inputs = V_{INH}.
3. Maximum gain change from T_A = +25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
4. Digital inputs = V_{INH}, V_{DD} = +14V to +17V.
5. Guaranteed and not tested.
6. Digital inputs = V_{INL}.
7. Digital inputs = V_{INH}.
8. Settles to 0.05% FSR; R_{LOAD} = 100Ω; digital inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}.
9. AC parameters sample tested to ensure spec compliance.
10. Digital input = V_{INL}; V_{REF} = $20V_{p-p}$, f = 100kHz Sinewave.
11. Absolute temperature coefficient is approximately +50ppm/°C.
12. All grades guaranteed monotonic.

DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.591 × 2.540 mm, 6.58 sq. mm)

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT BIT 1 (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT BIT 2
6. DIGITAL INPUT BIT 3
7. DIGITAL INPUT BIT 4
8. DIGITAL INPUT BIT 5
9. DIGITAL INPUT BIT 6
10. DIGITAL INPUT BIT 7
11. DIGITAL INPUT BIT 8
12. DIGITAL INPUT BIT 9
13. DIGITAL INPUT BIT 10 (LEAST SIGNIFICANT BIT)
14. POSITIVE POWER SUPPLY
15. REFERENCE INPUT VOLTAGE
16. INTERNAL FEEDBACK RESISTOR

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		10	Bits MIN
Relative Accuracy (Notes 1, 2)	INL		±0.1 (±1)	% FSR (LSB) MAX
Differential Nonlinearity (Note 10)	DNL		±0.1 (±1)	%FSR (LSB) MAX
Gain Error (Notes 2, 3, 4)	G_{FSE}		±1.4 (±14)	% FS (LSB) MAX
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$ (Notes 2, 5, 6)	PSR		0.005	%/% MAX
Output Leakage Current I_{OUT1} (Notes 2, 7)	I_{LKG1}		±50	nA MAX
Output Leakage Current I_{OUT2} (Notes 2, 8)	I_{LKG2}		±50	nA MAX
REFERENCE INPUT				
Reference Input Resistance (Notes 2, 9)	R_{IN}		5/20	kΩ MIN/MAX

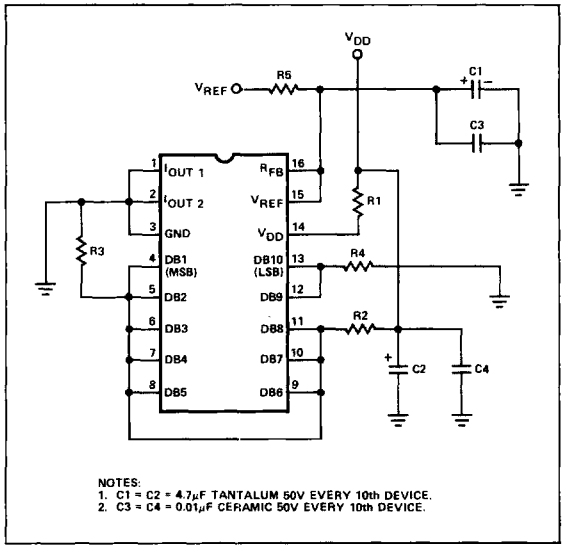
WAFER TEST LIMITS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V, T_A = +25°C, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
DIGITAL INPUTS				
Digital Input High (Note 2)	V_{INH}		2.4	V MIN
Digital Input Low (Note 2)	V_{INL}		0.8	V MAX
Input Leakage Current (Note 2)	I_{IN}	V_{IN} = 0V and V_{DD}	±1	µA MAX
POWER REQUIREMENTS				
Power Supply Voltage	V_{DD}		+15 ±10%	V MAX
Supply Current (Note 2)	I_{DD}	Digital Inputs = V_{NL} or V_{INH}	2	mA MAX

NOTES:
1. "FSR" is full-scale range.
2. DICE final electrical tests are: relative accuracy, gain error, output leakage current, V_{INH}, V_{INL}, PSR, R_{IN}, I_{IN} and I_{DD} at +25°C.
3. Full-scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$; Digital inputs = V_{INH}.
4. Maximum gain change from T_A = +25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
5. Digital inputs = V_{INH}, V_{DD} = +14V to +17V.
6. Guaranteed and not tested.
7. Digital inputs = V_{INL}.
8. Digital inputs = V_{INH}.
9. Absolute temperature coefficient is approximately +300ppm/°C.
10. Guaranteed monotonic.

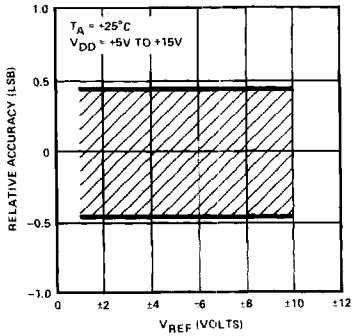
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

BURN-IN CIRCUIT

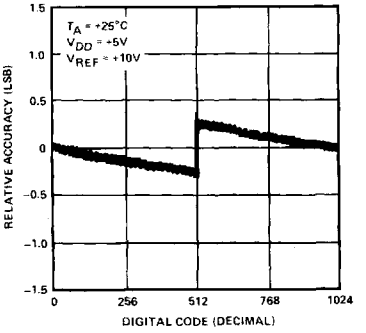


TYPICAL PERFORMANCE CHARACTERISTICS

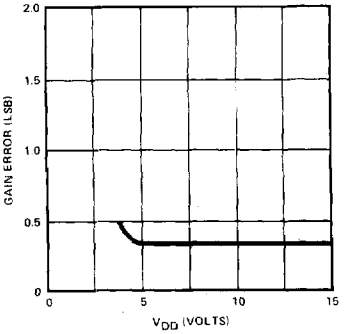
RELATIVE ACCURACY (NONLINEARITY) vs V_{REF}



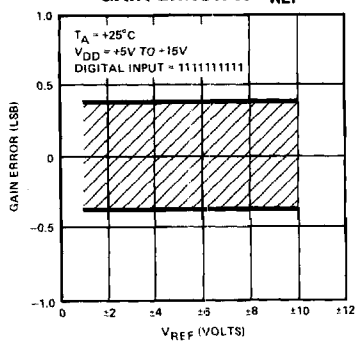
RELATIVE ACCURACY (NONLINEARITY) vs DIGITAL CODE



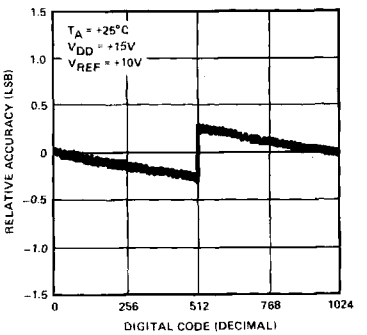
GAIN ERROR vs SUPPLY VOLTAGE



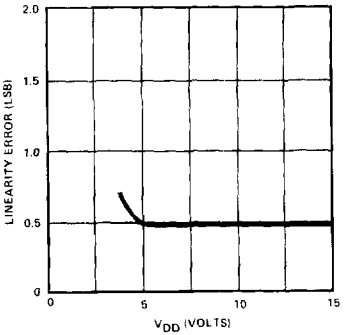
GAIN ERROR vs V_{REF}



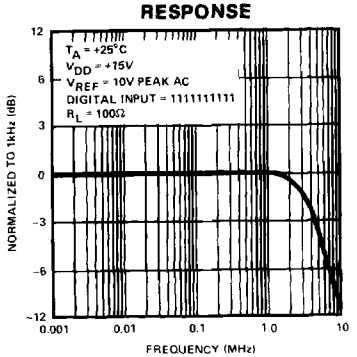
RELATIVE ACCURACY (NONLINEARITY) vs DIGITAL CODE



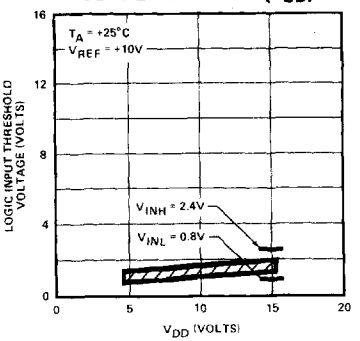
LINEARITY ERROR vs SUPPLY VOLTAGE



V_{REF} FREQUENCY RESPONSE



LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



DEFINITIONS

RESOLUTION
The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY
Relative accuracy or end-point (nonlinearity) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

SETTLING TIME
Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN
Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output.

FEEDTHROUGH ERROR
Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE
Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT
Current which appears on I_{OUT1} terminal with all digital inputs low or on I_{OUT2} terrninal when all inputs are high.

CIRCUIT DESCRIPTION
The PM-7533 is a 10-bit multiplying D/A converter. It consists of a silicon-chrome thin-film R-2R resistor ladder network and ten pairs of NMOS current steering switches, all on a monolithic chip. The NMOS current steering switches are controlled by CMOS inverters. Most applications require the addition of only an operational amplifier and a current or voltage reference.

An inverted R-2R ladder network in a simplified D/A converter circuit is shown in Figure 1. The current through each ladder leg is switched between I_{OUT1} and I_{OUT2} under the control of the digital inputs. This allows a constant current to be maintained in each ladder leg regardless of the digital-input switch states.

The design incorporates a matching MOS transistor in series with the feedback and terminating resistors. These MOS transistors, shown as switches in Figure 1, provide improved gain and linearity performance over the operating temperature range. The resulting typical gain temperature coefficient is 2ppm/°C.

FIGURE 1: Simplified DAC Circuit

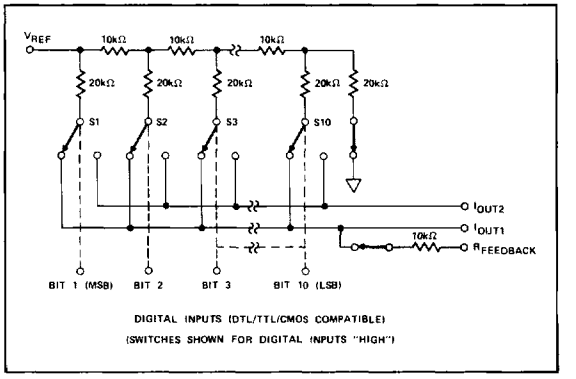
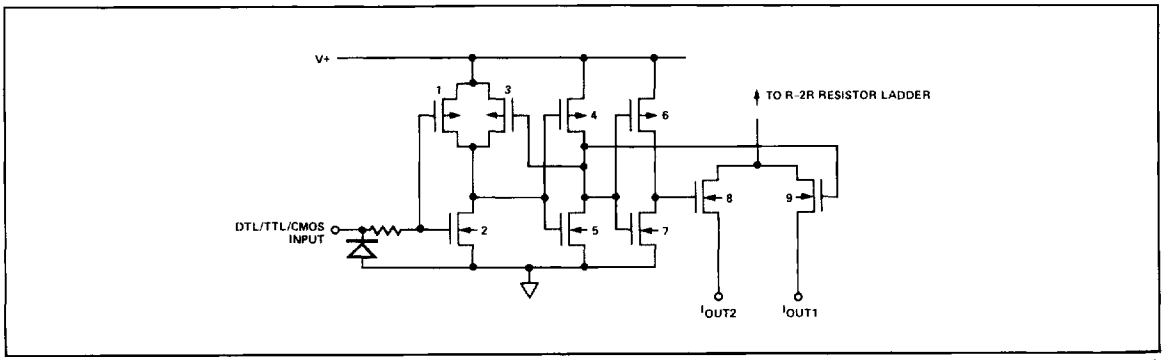


Figure 2 shows one of ten digital input CMOS inverters driving an NMOS switch. The size of devices 1, 2, and 3 are optimized to make the digital inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives the two inverters (4, 5) and (6, 7), which drives the two NMOS switches (8 and 9). The switch "ON" resistances are binarily-scaled so that the voltage drop across each switch is the same; that is, switch S1 in Figure 1 (8 and 9 of Figure 2) was designed for an "ON" resistance of 20 ohms, switch S2 for 40 ohms, etc. With a 10V reference input, switch S1 current is 0.5mA, switch S2 is 0.25mA, etc. This will maintain a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal so that the D/A converter accuracy is maintained.

FIGURE 2: CMOS Switch



EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits of the DAC with all digital inputs high and low respectively. With all digital inputs in the high state as shown in Figure 3, the reference current is switched to the I_{OUT1} terminal, and the I_{OUT2} terminal is open-circuited. Only the output capacitance, surface, leakages, and junction leakages appear at the I_{OUT2} terminal. The 1/1024 current source is a constant 1-bit current drain through the termination resistor of the R-2R ladder network. The $I_{LEAKAGE}$ current source represents a combination of surface and junction leakages to the substrate. The "ON" capacitance of the output NMOS switch is higher on the I_{OUT1} terminal when all digital inputs are high (MOS transistor gate capacitance increases with applied gate voltage).

FIGURE 3: Equivalent DAC Circuit (All digital inputs HIGH).

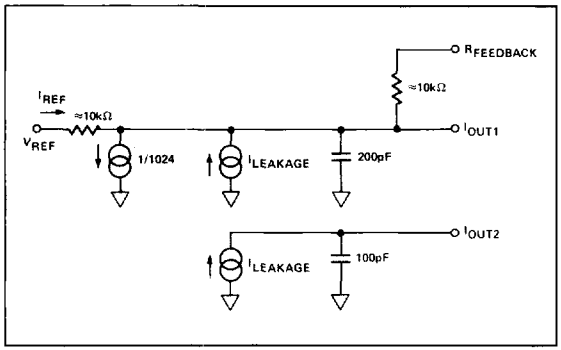
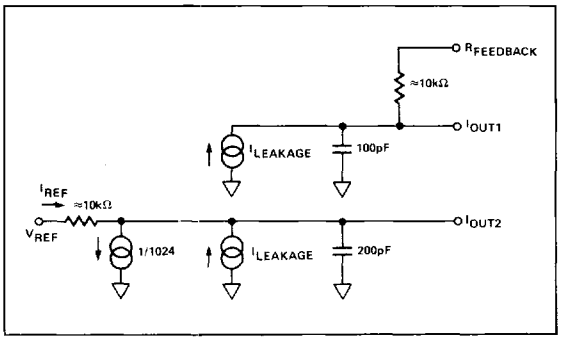


FIGURE 4: Equivalent DAC Circuit (All digital inputs LOW).



When the conditions are reversed with all digital inputs low as shown in Figure 4, the I_{OUT1} terminal is open-circuited and the current is directed towards the I_{OUT2} terminal.

APPLICATIONS INFORMATION

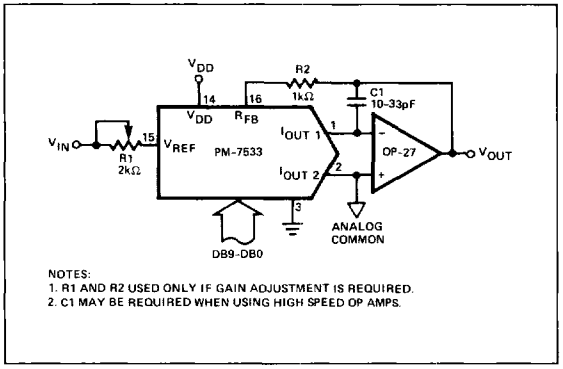
Figure 5 shows a simple unipolar circuit using the PM-7533. Resistors R1 and R2 are used to trim for full scale. Full-scale output voltage = $-V_{REF} \times (1023/1024)$ with all digital inputs high. Full scale can also be adjusted using V_{REF} thereby eliminating resistors R1 and R2. In many applications, R1 and R2 are not required. Zero-scale output voltage (with all digital inputs low) should be adjusted to less than 10% of 1 LSB using the op amp offset adjust. This will help to keep the nonlinearity errors to a minimum. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high-speed op amps.

The circuit of Figure 5 can be used either as a fixed reference digital-to-analog converter, or can be used with an AC signal at the V_{REF} terminal. Used with a fixed reference voltage, the output voltage range will be from zero to $-V_{REF}$, (the op amp inverts the voltage). The circuit behaves as an attenuator when used with an AC V_{REF} signal. The input voltage range is ±20V, but this voltage will be limited by the op amp voltage range. The digital-input-code versus analog-output-voltage is shown is Table 1. The transfer function is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \cdots \frac{A_{10}}{2^{10}}\right)$$

where $A_1 \ldots A_{10}$ assumes a value of 1 for an ON bit and 0 for an OFF bit.

FIGURE 5: Unipolar Binary Operation (2-Quadrant Multiplication)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 MAY BE REQUIRED WHEN USING HIGH SPEED OP AMPS.

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right) = \frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:
1. Nominal full scale for the circuit of Figure 5 is given by
   $FS = -V_{REF}\left(\frac{1023}{1024}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 5 is given by
   $LSB = V_{REF}\left(\frac{1}{1024}\right)$ or $V_{REF}(2^{-n})$.

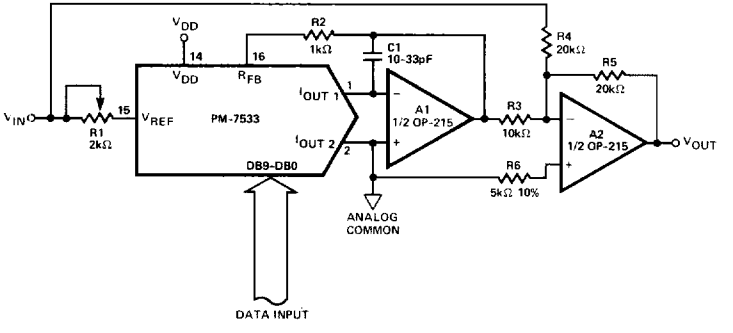
Figure 6 shows a simple bipolar output circuit using the PM-7533 and a PMI OP-215 dual op amp. The circuit uses offset binary coding and a fixed DC voltage for V_{REF}. Digitally-controlled attenuation of an AC signal occurs when the signal is used as the signal source at V_{REF}. Negative output full-scale is adjusted by setting the digital inputs to all zeros and adjusting the value of the V_{REF} voltage or R5. The zero-scale output voltage is adjusted while the digital inputs are set to 1000000000 and adjusting R1 for a zero output voltage (less than 10% of 1 LSB). Resistors R3, R4 and R5 must be selected for matching and tracking in order to keep offset and full scale errors to a minimum. Resistors R1 and R2 temperature coefficients must be taken into account if they are used. C1 phase compensation capacitor may not be needed and should be selected empirically. The digital input code versus analog output voltage is shown in Table 2.

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{512}\right)$

NOTES:
1. Nominal full scale for the circuit of Figure 6 is given by
   $FSR = V_{REF}\left(\frac{512}{512}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 6 is given by
   $LSB = V_{REF}\left(\frac{1}{512}\right)$.

FIGURE 6: Bipolar Operation (4-Quadrant Multiplication)



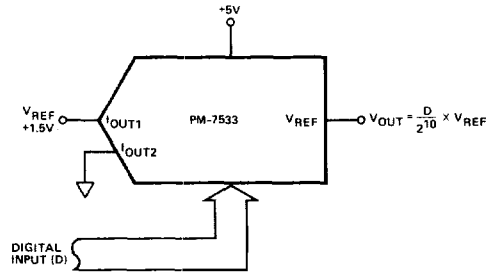
The PM-7533 may be used in the voltage output operation as shown in Figure 7. This circuit configuration will lend itself to single-supply operation because signal inversion does not occur. The output should be buffered due to its high output resistance (10kΩ) to prevent loading errors. The reference voltage should be kept to +1.5 volts maximum to keep nonlinearity errors to less than 1 LSB as shown in Figure 8.

By connecting the DAC in the feedback of an op amp as shown in Figure 9, the circuit behaves as a programmable gain amplifier (analog/digital divider). The transfer function is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \cdots \frac{A_{10}}{2^{10}}} \right)$$

where $A_1 \ldots A_{10}$ assumes a value of 1 or 0.

FIGURE 7: Voltage Output Operation



NOTES:
1. $V_{REF} \leq +1.5V$ TO KEEP NONLINEARITY ERRORS < 1 LSB.
2. $R_{OUT} \approx 10k\Omega$. THIS HIGH OUTPUT RESISTANCE SHOULD BE BUFFERED TO PREVENT LOADING ERRORS.
3. THIS CIRCUIT WILL LEND ITSELF TO SINGLE SUPPLY OPERATION.

FIGURE 8: Voltage Mode

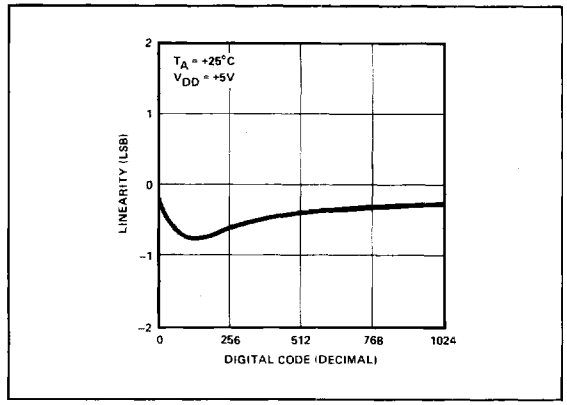
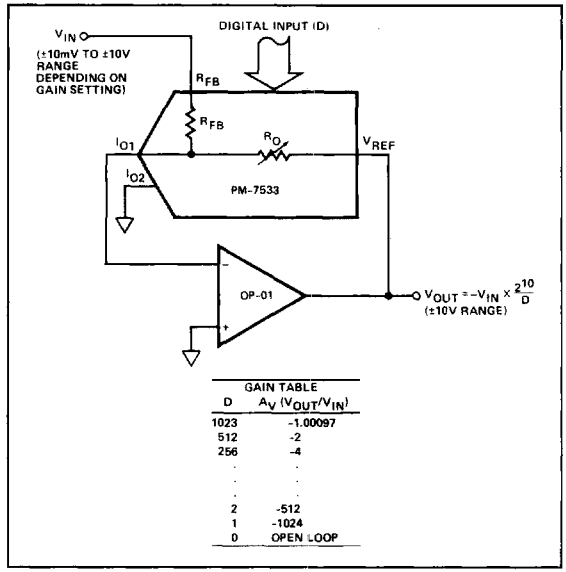


FIGURE 9: Programmable Gain Amplifier



GAIN TABLE

D	A_V (V_{OUT}/V_{IN})
1023	-1.00097
512	-2
256	-4
.	.
.	.
.	.
2	-512
1	-1024
0	OPEN LOOP